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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
10/046,759	01/17/2002	Atsushi Watanabe	100353-00093	2648	
	7590 04/26/2007 KINTNER PLOTKIN & K	AHN PLLC	EXAM	INER	
Suite 600 CERVETTI, DAVID GARG		AVID GARCIA			
1050 Connectic Washington, De	cut Avenue, N.W. C 20036-5339		ART UNIT PAPER NUMBER		
			2136		
SHORTENED STATUTOR	Y PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE		
3 MO	NTHS	04/26/2007	PAI	PER	

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

	Application No.	Applicant(s)		
	10/046,759	WATANABE ET AL.	WATANABE ET AL.	
Office Action Summary	Examiner	Art Unit		
	David G. Cervetti	2136		
The MAILING DATE of this communication appeared for Reply	pears on the cover sheet w	ith the correspondence address -		
A SHORTENED STATUTORY PERIOD FOR REPL WHICHEVER IS LONGER, FROM THE MAILING D. - Extensions of time may be available under the provisions of 37 CFR 1.1 after SIX (6) MONTHS from the mailing date of this communication. - If NO period for reply is specified above, the maximum statutory period. - Failure to reply within the set or extended period for reply will, by statute Any reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b).	PATE OF THIS COMMUNI 136(a). In no event, however, may a will apply and will expire SIX (6) MO e, cause the application to become A	CATION. reply be timely filed NTHS from the mailing date of this communicated BANDONED (35 U.S.C. § 133).	·	
Status				
 1) ⊠ Responsive to communication(s) filed on 24 J 2a) ☐ This action is FINAL. 2b) ⊠ This 3) ☐ Since this application is in condition for allowated closed in accordance with the practice under the condition of the con	s action is non-final. ance except for formal mat		s is	
Disposition of Claims				
 4) Claim(s) 1-10 is/are pending in the application 4a) Of the above claim(s) is/are withdra 5) Claim(s) is/are allowed. 6) Claim(s) 1-10 is/are rejected. 7) Claim(s) is/are objected to. 8) Claim(s) are subject to restriction and/or contents. 	wn from consideration.			
Application Papers				
9) ☐ The specification is objected to by the Examine 10) ☒ The drawing(s) filed on 17 January 2002 is/are Applicant may not request that any objection to the Replacement drawing sheet(s) including the correct 11) ☐ The oath or declaration is objected to by the E	e: a) accepted or b) ce drawing(s) be held in abeyaction is required if the drawing	nce. See 37 CFR 1.85(a). g(s) is objected to. See 37 CFR 1.12		
Priority under 35 U.S.C. § 119		•		
a) Acknowledgment is made of a claim for foreign a) All b) Some * c) None of: 1. Certified copies of the priority document 2. Certified copies of the priority document 3. Copies of the certified copies of the priority document application from the International Bureat * See the attached detailed Office action for a list	ts have been received. Its have been received in Abority documents have been au (PCT Rule 17.2(a)).	Application No In received in this National Stage		
Attachment(s) 1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)		Summary (PTO-413) (s)/Mail Date		
3) Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date	5) Notice of Other:	Informal Patent Application	,	

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DETAILED ACTION

1. Applicant's arguments filed January 24, 2007, have been fully considered but are not persuasive.

2. Claims 1-10 are pending and have been examined.

Response to Amendment

3. Applicant's arguments with respect to the prior art have been considered but are moot in view of the new ground(s) of rejection.

Continued Examination Under 37 CFR 1.114

4. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114.

Claim Rejections - 35 USC § 102

- 5. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.
- 6. Claims 1-9 are rejected under 35 U.S.C. 102(e) as being anticipated by Parlour et al. (US Patent 6,904,527, hereinafter Parlour).

Regarding claim 1, Parlour teaches a semiconductor integrated circuit (col. 6, lines 30-64), comprising:

- a plurality of internal hardware function blocks provided inside the semiconductor integrated circuit (col. 6, lines 30-64);

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- a nonvolatile memory unit which stores therein coded license information indicative of a usable/unusable status separately for each of the plurality of internal hardware function blocks (col. 6, lines 30-64, col. 7, lines 8-40); and

a decoder circuit which decodes the license information stored in said nonvolatile memory unit, and makes each of the internal hardware function blocks separately either usable or unusable depending on the decoded license information (col. 7, lines 40-67, col. 8, lines 1-16).

Regarding claim 2, Parlour teaches a status unit that has at least part of the decoded license information stored therein in such a manner as to be accessible from an exterior of said semiconductor integrated circuit (col. 8, lines 40-67).

Regarding claim 3, Parlour teaches a calendar circuit which indicates a current date and time, wherein said decoder circuit makes said plurality of hardware function blocks usable in response to a finding that the current date and time indicated by the calendar circuit is within a valid period indicated by the decoded license information, and makes said plurality of hardware function blocks unusable in response to a finding that the current date and time indicated by the calendar circuit is after a valid period indicated by the decoded license information (col. 6, lines 45-63).

Regarding claim 4, Parlour teaches a counter circuit that counts a number indicative of how many times said plurality of hardware function blocks are used, wherein said decoder circuit makes said plurality of hardware function blocks usable in response to a finding that the number counted by said counter circuit is within a number of valid use indicated by the decoded license information, and makes said plurality of

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hardware function blocks unusable in response to a finding that the number counted by said counter circuit exceeds the number of valid use indicated by the decoded license information (col. 6, lines 45-63, col. 11, lines 1-30).

Regarding claim 5, Parlour teaches a license encoder circuit which encodes the number counted by said counter circuit, wherein the number encoded by said license encoder circuit is stored in said nonvolatile memory unit as updated license information (col. 6, lines 45-63, col. 11, lines 1-30).

Regarding claim 6, Parlour teaches wherein coding and decoding of the license information is encrypting and decrypting that prevent the license information in said nonvolatile memory unit from being illegally rewritten (col. 9, lines 20-62).

Regarding claim 7, Parlour teaches wherein said decoder circuit includes: a decoder which decodes the license information stored in said nonvolatile memory unit; a license register which stores therein the decoded license information decoded by said decoder; and a control circuit which makes said plurality of hardware function blocks either usable or unusable depending on the information stored in said license register (col. 9, lines 20-62, col. 11, lines 1-30)

Regarding claim 8, Parlour teaches wherein said control circuit controls a chip enable signal of said plurality of hardware function blocks in order to make said plurality of hardware function blocks either usable or unusable (col. 9, lines 20-62, col. 11, lines 1-30).

Regarding claim 9, Parlour teaches wherein said control circuit controls a clock signal of said plurality of hardware function blocks in order to make said plurality of

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hardware function blocks either usable or unusable (col. 9, lines 20-62, col. 11, lines 1-30).

Regarding claim 10, Parlour teaches wherein said nonvolatile memory unit receives the coded license information from an external large scale integration (LSI) tester, and no external pin is provided for a purpose of receiving the coded license information (col. 3, lines 39-63).

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Conclusion

- 7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Roohparvar (US Patent 6,438,068) teaches enabling/disabling a hardware/software block.
- 8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David G. Cervetti whose telephone number is (571)272-5861. The examiner can normally be reached on Monday-Tuesday and Thursday-Friday.
- 9. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nasser Moazzami can be reached on (571)272-4195. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.
- 10. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NASSER MOAZZAMI SUPERVISORY PATENT EXAMINER TECHNOLOGY CENTER 2100

DGC